The solid lines indicate the flow of digital data, and the dot lines indicate the flow of control signals.

The action of each unit will be described as follows.

When error correction begins, the initial setting unit 103 writes the data of the first sector to the first buffer memory 41 and the data of the second sector to the second buffer memory 42. The initial setting unit 103 also sets the flag in the buffer switch control unit 101 at 1, and provides the buffer switch control unit 101 and the buffer data transfer control unit 102 with instructions for the setting.

The buffer switch control unit 101, when the error correction begins, refers to the flag, and connects the first buffer memory 41 with the syndrome calculator 5, the error detector 7, and the like. As the error correction proceeds, the buffer switch control unit 101 refers to the flag every time it receives a transfer signal from the buffer data transfer control unit 102 to switch the buffer memories, and write data received from the upstream processing unit 10 to the corresponding buffer memory every time the flag is switched.

Every time error correction for one sector is complete, the buffer data transfer control unit 102 switches circuits so as to transfer data either in the first buffer memory 41 or the second buffer memory 42 to the downstream processing unit 9; transmits a transfer signal to the buffer switch control unit 101 at the same time; and makes the flag switch unit set the flag between at 1 and at 2 alternately.

When the error correction for one sector is complete, the data in the buffer memory that has been in process is flown to the downstream

processing unit 9. On the other hand, the data to be subjected to the next error correction are already written in the other buffer memory by the buffer switch control unit 101, which quickens error correction.

(Embodiment 5)

While in Embodiments 1 to 3, the mid-term result register 8 is shared by all sectors, in the present embodiment each of the 16 sectors of one ECC block is provided with a mid-term result register, considering that data are often transferred in one-ECC increments in the actual error correction, which may include vertical error correction.

Figure 12 shows the structure of the error correction device 100 of the present embodiment. In Figure 12, an optical disk 201 is driven by a spindle motor 202, and an optical head 203 reads data stored in the optical disk 201 and outputs them to an amplifier 204. An reception code 29 is read out in the same direction as the horizontal (inner code) error correction and entered to the error correction device 100. In the device 100, the reception code 29 is entered to a demodulator 10 and the demodulated code is stored in the buffer memory 4 by a demodulation code enter signal 25 outputted from the bus control unit 3.

A transfer control unit 9 transmits an error-corrected code 30 read from the buffer memory 4 to an external unit 205 such as a personal computer. The data transfer to the external unit 205 is performed by the buffer memory access signal 14 and a demodulation code enter signal 25, which are outputted by the bus control unit 3.

As shown in Figure 12, the error detector 7 is provided with 16 mid-term result registers 801, 802, ... 816 for 16 sectors in one ECC block.

Figure 13 shows error-containing codes in the sectors and the data transfer range in error detection of the present embodiment.

The behavior of the error correction device 100 of the present embodiment thus structured will be described with reference to Figures 12, 13, and 14.

Step (e-1): in order to perform error correction, the system control unit 1 outputs the DMA command 12 to the DMA control unit 2 so as to provide instructions to transfer data equivalent to one code word in the horizontal direction×13 times, or one sector from the buffer memory 4 to the syndrome calculator 5 and to the error detector 7.

Step (e-2): the DMA control unit 2 outputs the DMA request 13 to the bus control unit 3 so as to request the data transfer from the buffer memory 4 to the syndrome calculator 5 and to the error detector 71.

Step (e-3): the bus control unit 3 puts the data bus 11 in commission, and outputs the buffer memory access signal 14 to the buffer memory 4. The bus control unit 3 then outputs the syndrome data supply signal 15 and the error detector data supply signal 20 to the syndrome calculator 5 and the error detector 7, respectively, so as to supply the data read from the buffer memory 4 to the syndrome calculator 5 and to the error detector 7.

Step (e-4): the syndrome calculator 5 calculates a syndrome 16 of the transferred horizontal code word, and outputs the syndrome 16 to the error corrector 6. If the code word contains an error-containing code, or if the syndrome is not zero, the syndrome calculator 5 outputs the error-containing code detection signal 22 to the error corrector 7 and to the